REMARKS

Claims 1-50 are pending in this application. In the Office Action dated September 9, 2005, the Examiner took the following action: (1) objected to claims 1-50 for informalities; (2) rejected claims 1-6, 13-19, 40-44 and 50 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,638,534 to Mote et al. ("Mote"); (3) rejected claims 7-11, 20-24 and 45-49 under 35 U.S.C. § 103(a) as being unpatentable over Mote in view of U.S. Patent No. 5,796,413 to Shipp et al. ("Shipp"); (4) rejected claims 12 and 25 under 35 U.S.C. § 103(a) as being unpatentable over Mote in view of U.S. Patent Publication No. 2002/0178319 to Sanchez-Olea ("Sanchez-Olea"); (5) rejected claims 26-31 and 38 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,496,193 to Surti et al. ("Surti") in view of Mote; (6) rejected claims 32-36 under 35 U.S.C. § 103(a) as being unpatentable over Surti in view of Mote and further in view of Shipp; and (7) rejected claims 37 and 39 under 35 U.S.C. § 103(a) as being unpatentable over Surti in view of Mote and further in view of Sanchez-Olea.

The Examiner has indicated claims 1-50 are objected to because it is unclear how one could "couple(d)" or be "coupling" memory requests. Examiner has requested appropriate correction or clarification. Claims 1-50 have been amended to replace "couple(d)" with "transmit(ted)" and "coupling" with "transmitting" where appropriate. In some instances it is proper to use "couple" and "coupling." For example, it is proper to couple two ports together, such as an input and output port, and an electrical element may be "coupled to receive" a particular signal. In other instances, such as in claim 8, the terms "couple(d)" and "coupling" were not included in the claim language.

Before discussing the merits of this rejection, the disclosed embodiments of the invention will now be discussed in comparison to the cited references. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences merely help the examiner appreciate important claim distinctions discussed thereafter.

The disclosed invention is directed to memory modules having posted write buffers and methods of posting write requests in memory modules. In a conventional computer

system, the processor issues a memory request such as a read command and an address designating the location from which data or instructions are to be read. A memory controller may then be used to generate appropriate command and address signals, which are applied to the system memory. While the operating speed of memory devices has continuously increased, the operating speed of memory controllers coupling processors to memory devices has not kept pace. Therefore, despite memory devices outputting at a high data rate, the delay in providing the data can significantly slow the operating speed of the computer system. Additionally, if a controller issues a write request after a read request or another write request, the respective memory device may not be able to respond to the write request until after the read request or earlier write request has been serviced.

Attempts have been made to eliminate this memory latency problem by having posted write buffers to store write requests while a read request or a prior write request is being serviced. In these computer systems, memory requests can be serviced out of order and a write request can be stored in the posted write buffer while a subsequent read request is being serviced. Also, a write request may be stored in the posted write buffer while a read request or an earlier write request is being serviced. Additionally, a series of write requests may be stored in the posted write buffer, for example, to allow the read requests to be serviced in a pipelined manner followed by servicing the stored write requests in a pipelined manner. However, while a posted write buffer in a convention computer system is capable of handling the write requests that a processor issues to several memory devices, it is not likely adequate for a memory system using a hub architecture. In a hub architecture, a processor is coupled to several memory modules through a system controller or similar device. Each memory module includes a memory hub coupled to the controller and to several memory devices within the memory module. A posted write buffer located in the controller would require that each of the write memory requests be stored in the controller until a memory device in a memory module was able to service the write request. The controller would therefore have to keep track of the operation of each memory device, such as by receiving signals from the memory hubs indicating when each memory device was available to service the next write memory request. Therefore, there is a need for a posted write buffer in a computer system that is specially adapted to take advantage of the high bandwidth and low latency provided by a memory hub architecture.

In an embodiment of the present invention, a computer system includes a processor and system controller serving as a communications path to the processor and a variety of other components within the computer system. More importantly, the system controller is coupled to several memory modules, ideally by a high speed link which may be an optical or electrical communication path. Each memory module includes a memory hub for controlling access to a plurality of memory devices. The memory hub may include a link interface that is coupled to the high-speed link, and may be used to store memory requests until they can be processed by the memory hub. The memory hub also includes a posted write buffer for storing write requests, and a conventional coherency circuitry for processing read requests. The posted write buffer is coupled to a multiplexer and a memory sequencer, which are both coupled to a memory device interface. The multiplexer, memory sequencer, and memory device interface work in concert with the posted write buffer to process or store read and write memory requests accordingly, and including such requests as the "read around write" requests. By placing a posted write buffer in a memory hub on each of the memory modules, the controller connected to each of the memory modules can simply transmit write requests to the memory modules as fast as they are received from the processor. It is not necessary for the controller to store write memory requests or to keep track of when memory devices in the memory modules are free to service the next write request as in the prior art controllers discussed above.

The primary reference cited in the Office Action is the patent to Mote, which describes essentially the same type of memory sub-system discussed in the "Background" section of this application. The memory system includes a memory controller and a plurality of dynamic random access memories. The memory controller includes a posted write buffer, and is designed to reduce the memory access time for read and write cycle access requests in a memory sub-system with page mode accesses. The memory controller as described by Mote enables the rearrangement of the write and write memory requests to, for example, perform all reads before all writes. A number of embodiments of the memory controller are described by Mote. In all of these embodiments, the memory controller controls access to dynamic random access memory devices to reduce the overall memory access time. In all of these embodiments, the memory controller must keep track of when a memory device is free to service the next write memory access stored in the memory controller. The memory controller is not free to simply issue write

memory requests to the memory modules as fast as they are received from the processor. None of these embodiments include a primary system controller coupled to a plurality of memory modules each of which includes a memory hub containing a posted write buffer storing write memory accesses that are transmitted to memory devices in each of the memory modules. As explained above, while the memory controller of Mote may reduce the overall memory access time to a set of memory devices to which the memory controller is directly connected, it would not allow a memory system to achieve all of the advantages inherent in a memory hub architecture.

Turning now to the claims, the anticipation rejection of claim 1 under U.S.C. §102(b) should be withdrawn because the Mote patent does not disclose the claimed invention exactly as specified in the claim. The patent to Mote discloses a memory sub-system using a posted write buffer located in the memory controller as is known in the art. The Mote patent does not describe the memory subsystem 120 as being in the form of a module that is physically separate from the rest of the computer system 100 disclosed in the Mote patent. As is well known in the art, a memory module has a modular construction, such as a single in-line memory module ("SIMM") and double in-line memory module ("DIMM"). Where components in the Mote system 100 are, in fact, packaged together as a module, such as the "CPU module 110," they are specifically described as a "module." If Mote's memory sub-system 120 was packaged together as a module, the Mote patent would have described it as a module just as it did with the CPU module 110.

As is also well-known in the art, a memory module is connected to a controller or similar device rather than directly to a processor or CPU. In contrast, the memory controller 130 in the memory subsystem of Mote is connected directly to the CPU module 110. Mote's memory system 120 is, therefore, clearly not a "memory module" as specified in claim 1.

Claim 14, which has also been rejected as being anticipated by the Mote patent, has been amended to more clearly distinguish over the prior art. Amended claim 14 specifies a memory hub having a link interface structured to receive memory requests *from a controller*. The memory hub also includes a memory device interface, a posted write buffer, and a read request path operable to transmit read memory requests to the memory device interface. To the extent that Mote's memory controller can be considered a memory hub, it does not receive

memory requests from a controller. Instead, it is a controller, and it receives memory requests directly from a CPU module 110.

The Mote patent also fails to anticipate the "method of reading data from a plurality of memory modules" specified in claim 40. In fact, as explained above, the Mote patent does not even describe the existence of memory modules in the disclosed computer system 100. Nevertheless, applicant is amending claim 40 to better distinguish over the Mote patent. Claim 40 now specifies the received memory requests are received from a "controller." In contrast, the memory controller 130 of Mote receives memory requests from the CPU module 110. Claim 40 is therefore clearly novel over the Mote patent.

The only remaining independent claim is claim 26, which is directed to a computer system having a system controller coupled to a CPU and to a plurality of memory modules. Each of the memory modules have a plurality of memory devices and a memory hub that contains, inter alia, a posted write buffer. Claim 26 has been rejected as being obvious over the patent to Surti in view of the patent to Mote. The Surti patent discloses a computer system having a processor 11 coupled to a memory controller 12, which is in turn connected to DRAM system memory 14. The Office Action admits that the Surti patent does not disclose memory modules having a memory hub connected to a plurality of memory devices. However, it is argued that the Mote patent provides these teachings that are missing from the Surti patent. In actuality, the Mote patent provides exactly the same teachings as the Surti patent, namely a controller coupled between a CPU and memory devices. Therefore, the Mote patent does not supply the teachings that are missing from the teaching of the Surti patent.

Even if the Mote patent had, in fact, described the disclosed memory system 120 as being a memory module (which, as explained above, it does not), the combination of the Surti patent and the Mote patent would still not suggest a memory hub connected to memory devices and to a controller. If Mote had taught placing the controller on a memory module with the memory devices, that teaching would, at best, suggest relocating the controller in the Surti patent to a memory module as taught by Mote. There would still be no teaching of using both a memory hub *and* a controller. The obviousness rejecting of claim 26 is apparently based on the contention that the DRAMs 135 *and* memory controller 130 and of Mote would be used in place of the DRAM system memory 14 of Surti so that the resulting system would have two memory

controllers. However, neither reference suggests why it would be desirable to have two controllers in a computer system, the first connected to the CPU and the second connected to the first controller. In other words, the references whether taken alone or in combination fail to suggest coupling memory requests from a CPU to a first controller, and from a first controller to a second controller, and then from the second controller to the memory devices. For all of these reasons, the obviousness rejection of claim 26 should be withdrawn.

Accordingly, independent claims 1, 14, 26 and 40 should be allowable over the cited references. Claims depending from claims 1, 14, 26 and 40 should also be allowable because they depend from an allowable base claim and because of the additional limitations recited in the dependent claims.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,
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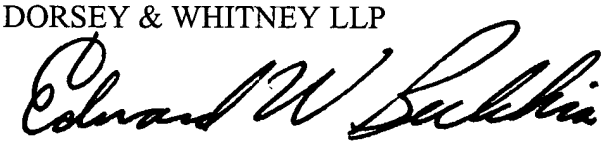

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